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# Fast Cyclic Redundancy Check (CRC) Generation



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## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to the field of data processing. More specifically, the present invention relates to high speed cyclic redundancy check (CRC) generation, having special application to high speed network traffic routing, such as Gigabit Ethernet packet switching.

### 2. Background Information

Cyclic Redundancy Check (CRC) has long been employed as a metric to detect transmission errors. The technique is employed in a wide variety of data processing related disciplines, including in particular, networking. The underlying mathematics including the polynomial divisions involved in the generation of a CRC value for a data block is well understood among those ordinarily skilled in the art. Various hardware as well as software implementations are known. Examples of known hardware implementations include but are not limited to the implementations available from e.g. Actel of Sunnyvale, CA.

With advances in integrated circuit, microprocessor, networking and communication technologies, increasing number of devices, in particular, digital computing devices, are being networked together. Devices are often first coupled to a local area network, such as an Ethernet based office/home network. In turn, the local area networks are interconnected together through wide area networks, such

as SONET, ATM, or Frame Relay networks, and the like. Of particular notoriety is the TCP/IP based global inter-networks, Internet.

As a result of this trend of increased connectivity, increasing number of applications that are network dependent are being deployed. Examples of these network dependent applications include but are not limited to, email, net based telephony, world wide web and various types of e-commerce. Successes of many of these content/service providers as well as commerce sites depend on high speed delivery of a large volume of data. As a result, high speed networking, which in turn translates into high speed CRC generation is needed.

Unfortunately, the current generation of CRC generators known in the art are generally unable to meet the speed requirement of the next generation IC based high speed network traffic routing devices. For these IC based devices, it is not only necessary for the CRC generation resource to be sufficiently fast to keep pace with the processing of a single network traffic flow, it is further desirable that the CRC generation resource to be sufficiently efficient and fast, such that it can be shared among the various flow processing units, thereby eliminating the need to have dedicated CRC generation resource for each of the flow processing units.

Thus, a highly efficient approach to CRC generation is needed.

## SUMMARY OF THE INVENTION

A CRC generation unit includes a number of CRC calculation assemblies to be selectively employed to incrementally calculate a CRC value for a sequence of N data bytes. The calculation is iteratively performed, one iteration at a time. Further,

the selection of the CRC calculation assemblies is made in accordance with the group size of each of a number of data word groups of the N data bytes.

In one embodiment, the CRC calculation assemblies include a first assembly to incrementally calculate the CRC value for an iteration, whenever the group size for the iteration is n/2 bytes or less, and a second assembly to incrementally calculate the CRC value for an iteration, whenever the group size for the iteration is more than n/2 bytes.

In one embodiment, the CRC generation unit is a shared resource to multiple network traffic flow processing units of a network traffic routing IC.

In one embodiment, the network traffic routing device is disposed on a single integrated circuit.

## BRIEF DESCRIPTION OF DRAWINGS

The present invention will be described by way of exemplary embodiments, but not limitations, illustrated in the accompanying drawings in which like references denote similar elements, and in which:

**Figure 1** illustrates an overview of the present invention;

**Figure 2** illustrates an example of packet data alignment or the lack thereof;

**Figure 3** illustrates one of the fast CRC generators of **Fig. 1** in further detail, in accordance with one embodiment;

**Figures 4a-4b** illustrate the 8-5 bytes CRC Calculator of **Fig. 3** in further detail, in accordance with two embodiments;

**Figures 5a-5b** illustrate the 4-1 bytes CRC Calculator of **Fig. 3** in further detail, in accordance with two embodiments; and

**Figur 6** illustrates an example routing device incorporated with the fast CRC generation teaching of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

In the following description, various aspects of the present invention will be described. However, it will be apparent to those skilled in the art that the present invention may be practiced with only some or all aspects of the present invention. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the present invention. However, it will also be apparent to one skilled in the art that the present invention may be practiced without the specific details. In other instances, well known features are omitted or simplified in order not to obscure the present invention. Further, the description repeatedly uses the phrase "in one embodiment", which ordinarily does not refer to the same embodiment, although it may.

### Overview

Referring now to **Figure 1**, wherein an overview of the present invention is illustrated. As shown, data sender **102** and data receiver **104** are coupled to each other via communication link **107**, over which data sender **102** may send data, including associated CRC values, to data receiver **104**. Both data sender **102** and data receiver **104** are equipped with fast CRC generator **106a/106b** of the present invention for generating CRC values for the data blocks being sent from data sender **102** to data receiver **104**. As will be described in more detail below, fast CRC generator **106a/106b** includes redundant circuit elements organized in accordance

with a parallel architecture to allow various calculations to be performed in an overlapped and parallel manner. As a result, fast CRC generator **106a/106b** may generate CRC values of variable length data blocks, such as variable length packet data, efficiently. In fact, experience has shown that fast CRC generator **106a/106b** is sufficiently efficient to allow fast CRC generator **106a/106b** to be shared by as many as 64 collections of network traffic flow processing resources of an IC based gigabit Ethernet routing device, resulting in a substantial net reduction in real estate requirement (notwithstanding the duplication of certain elements to enable the overlapped and parallel computations).

Except for fast CRC generator **106a/106b**, data sender **102**, data receiver **104** and communication link **107** are all intended to represent a broad range of data sending, data receiving and communication systems and/or components known in the art. Accordingly, except for fast CRC generator **106a/106b**, data sender **102**, data receiver **104** and communication link **107** will not be otherwise further described.

## Fast CRC Generator

**Figure 3** illustrates one of fast CRC generators **106a/106b** of **Fig. 1** in further details, in accordance with one embodiment. As illustrated, each fast CRC generator **106a/106b** includes three CRC calculation assembly and accumulator pairs **304** and **308a**, **306a** and **308b**, and **306b** and **308c** to facilitate overlapped CRC generation for two successive variable length series of data block groups. The CRC calculations are iteratively performed. Each fast CRC generator **106a/106b** further includes word extractor **302**, and selectors **310** and **312**, complementing the three CRC calculation assembly and accumulator pairs **304** and **308a**, **306a** and **308b**, and **306b** and **308c**. The elements are coupled to each other as shown.

Word extractor **302** is employed to extract data word groups from an input data stream. CRC calculation assembly and accumulator pair **304** and **308a** is employed to incrementally calculate the CRC value for a series of data word groups, for an iteration, whenever the group size of the extracted data word group for the iteration is more than n/2 data bytes, where n is an integer. Each of CRC calculation assembly and accumulator pairs **306a** and **308b**, and **306b** and **308c** is employed to incrementally calculate the CRC value for a series of data word groups, for an iteration, whenever the group size of the extracted data word group for the iteration is n/2 data bytes or less.

Selector **310** is employed to re-circulate an appropriate one of the accumulated calculation results stored in accumulator **308a-308c** to an appropriate one of calculation assemblies **304** and **306a-306b** for the next iteration. At the end of the calculation, selector **312**, in conjunction with selector **310**, facilitates selection of one of the accumulated calculation results stored in accumulator **308a-308c** to output or generate as the calculated CRC value.

The duplication of the CRC calculation resources for handling extract data word group with group sizes n/2 data bytes or less, advantageously enable the overlapping calculation of two CRC values for two successive series of data word groups. More specifically, it enables the current handling of the last data word group of a series of data words (e.g. a packet), and the first data word group of the next series of data words (e.g. the immediately following packet). [Note that it is impossible for both data word groups to have a group size of greater than n/2, and of course if one of the data word group has a group size greater than n/2, the group size of the other data word group necessarily is less than n/2. For the latter situation, no duplication of resources is necessary.]

Before describing the particular embodiment of CRC generator **106a/106b**, we refer first to **Figur 2**, wherein the alignment or the lack thereof, for successive variable length series of data block groups, such as variable length series of data packets, is illustrated. As shown, each variable length series of data block groups may be received through m groups of data word groups, where m is an integer equal to or greater than 1. The group size of each data word group may be 1, 2, 3 ... or n bytes, where n is also an integer. In various embodiments, n equals 8. For these embodiments, n/2 equals 4.

Referring back to **Fig. 2**, accordingly for the embodiments where n equals 8, CRC calculation assembly and accumulator pair **304** and **308a** is employed to incrementally calculate the CRC value for a series of data word groups, for an iteration, whenever the group size of the extracted data word group for the iteration is more than 4 data bytes (i.e. between 8 to 5 data bytes). Each of CRC calculation assembly and accumulator pairs **306a** and **308b**, and **306b** and **308c** is employed to incrementally calculate the CRC value for a series of data word groups, for an iteration, whenever the group size of the extracted data word group for the iteration is 4 data bytes or less (i.e. between 4 to 1 data bytes).



CRC Calculation Assembly (8 to 5 bytes)

**Figure 4a** illustrates CRC calculation assembly **304** of **Fig. 3** in further details, in accordance with one embodiment. As illustrated, CRC calculation assembly **304** includes four CRC calculators **402-408**, and a multiplexor **410**, coupled to each other as shown. Each of CRC calculators **402-408** is employed to handle the incremental calculation for an iteration for one of the group sizes. More specifically, CRC calculator **402** is employed to handle the incremental calculation for an iteration for a data word group with a group size of 8 bytes, CRC calculator

**404** is employed to handle the incremental calculation for an iteration for a data word group with a group size of 7 bytes, and so forth.

In other words, CRC calculation assembly **304** (for handling more than n/2 bytes calculations) has exactly n/2 CRC calculators. In each iteration, one of CRC calculators **402- 408** is selected for use (in accordance with the group size of the extracted data word group for the iteration).

Each CRC calculator **402**, **404**, **406** or **408** may be constituted with any one of a number of known CRC calculation circuitry, e.g. polynomial division circuitry.

**Figure 4b** illustrates CRC calculation assembly **304** of **Fig. 3** in further details, in accordance with another embodiment. As illustrated, CRC calculation assembly **304** includes input multiplexor **430**, three CRC calculators **422-426**, and multiplexors **432-434**, coupled to each other as shown. CRC calculators **422-426** are employed in combination at least some of the time to handle the incremental calculation for an iteration for one of the group sizes. More specifically, CRC calculator **422** is employed to handle the incremental calculation for an iteration for a data word group with a group size of 5 bytes, and CRC calculators **422** and **426** are employed in combination to handle the incremental calculation for an iteration for a data word group with a group size of 6 bytes. Similarly, CRC calculators **422** and **424** are employed to handle the incremental calculation for an iteration for a data word group with a group size of 7 bytes, and CRC calculators **402-406** are employed in combination to handle the incremental calculation for an iteration for a data word group with a group size of 8 bytes.

In other words, CRC calculation assembly **304** (for handling more than n/2 bytes calculations) has less than n/2 CRC calculators. In each of the iteration, for some data group sizes, CRC calculators **422-428** are employed in combination.

Similarly, each CRC calculator **422**, **424**, **426** or **428** may be constituted with any one of a number of known CRC calculation circuitry, e.g. polynomial division circuitry.

CRC Calculation Assembly (4 to 1 byte)

**Figure 5a-5b** illustrate CRC calculation assembly **306a/306b** of **Fig. 3** in further details, in accordance with one embodiment. As illustrated, in each embodiment, CRC calculation assembly **306a/306b** is similarly constituted as the corresponding embodiment of CRC calculation assembly **304**.

In other words, for the embodiment of **Fig. 5a**, CRC calculation assembly **306a/306b** (for handling n/2 bytes or less calculations) has exactly n/2 CRC calculators, as the embodiment of **Fig. 4a** for CRC calculation assembly **304**. In each iteration, one of CRC calculators **502**- **508** is selected for use (in accordance with the group size of the extracted data word group for the iteration). However, for the embodiment of **Fig. 5b**, CRC calculation assembly **306a/306b** (for handling n/2 bytes or less calculations) has less than n/2 CRC calculators, as the embodiment of **Fig. 4b** for CRC calculation assembly **304**. In each of the iteration, for some data group sizes, CRC calculators **522a**, **524b**, and **528** are employed in combination.

Likewise, each CRC calculator, **502-508** of **Fig. 5a**, and **522a-552b** and **524** of **Fig. 5b**, may be constituted with any one of a number of known CRC calculation circuitry, e.g. polynomial division circuitry.

Example Application

**Figure 6** illustrates an example application of the fast CRC generator of the present invention. As illustrated, data routing device **602** comprising receive interface **604** and transmit interface **612** is advantageously provided with a number

of per flow inbound processing units **606** and a number of per flow outbound processing functions **610**. Examples of these per flow inbound and outbound processing functions may include but are not limited to deciphering and ciphering functions. Additionally, data routing device **602** may also include a number of other common or shared function units **608**.

For the illustrated embodiment, common/shared function units **608** include in particular a shared CRC generation function block, incorporated with the fast CRC generator of **Fig. 3**. Accordingly, the common/shared CRC generator may alternate between generating CRC values for different data packets of the different flows being processed by per flow inbound/outbound processing units **608/610**.

As a result, the amount of storage required for provisioning the CRC function for the various flows being processed in parallel is substantially reduced under the present invention. In turn, data routing device **602** may be advantageously disposed on a single integrated circuit. Thus, data routing device **602** is able to handle high speed line rate data packet switching for multiple data flows at the same time. In one embodiment, data routing device **602** is an IC component for routing packets transmitted over an optical medium onto an electrical medium at very high speed.

## Conclusion and Epilogue

Thus, it can be seen from the above descriptions, a novel highly efficient method and apparatus for generating CRC for data blocks or data packets has been described. While the present invention has been described in terms of the above described embodiments, those skilled in the art will recognize that the invention is not limited to the embodiments described. The present invention can be practiced with modification and alteration within the spirit and scope of the appended claims. Thus,

the description is to be regarded as illustrative instead of restrictive on the present invention.

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